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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,627	BHARADWAJ ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

Claim 1 comprises steps of processing, selecting, allocating, determining, and the steps of attempting, treating, and scheduling under if conditions. The steps are just an abstract idea. The claim do not provide practical application that produces a useful, tangible and concrete result.

Therefore, the claim is non-statutory. Similarly, the further steps recited in Claims 2-11 do not produce a useful, tangible and concrete result. Similar problems exist in claims 12-22.

Claim Objections

3. Claims 23-46 are objected to because of the following informalities:

In claim 23 , line 7, "allocate register" should read - allocate a register -; and

In claim 35 , line 13, "allocate register" should read - allocate a register -.

Appropriate correction is required

Claim Rejections - 35 USC § 112

4. Claims 1-46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 5, it is not clear which operand "the operand" is referred to since at least two operands were

mentioned in lines 3 and 4 in the claim. Similar problems exist in claims 12, 23, and 35.

In claim 1, lines 5 and 6, a preserved register and a scratch register are allocated respectively. However, a register has already been allocated as mentioned in line 4. It is not clear why the registers are repeatedly allocated. Similar problems exist in claims 12, 23, and 35.

In claim 1, line 8, it is not clear what is meant by "treating the live range as tentative" since the values used in a computer system are all tentative. Something (such as that mentioned in claims 10, 21 or 34) are missing in the claim language. Similar problems exist in claims 12, 23, and 35.

In claim 1, line 9, it is not clear what will happen if the allocation was not successful. Similar problems exist in claim 12.

In claim 23, line 5, "the register allocation" lacks proper antecedent basis since it was not mentioned previously.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 7, 11-14, 18, 22, 34-37, 41, 45, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Srinivasan (U.S. Patent No. 6,651,247), herein referred to as Srinivasan'247.

Referring to claim 1, Srinivasan'247 discloses, as claimed, a method comprising: processing a group of instructions in topological dependence order (see Col. 2, line 61); selecting an instruction, associated with at least one operand, to schedule (by scheduler and register allocator 330, see Fig. 4); allocating (by scheduler and register allocator 330, see Fig. 4;

see also Col. 24, lines 30-45) a register (such as a static register 109 or rotating register 107 see Fig. 1; see also col. 28, lines 49-50 or 60-61) to one or more of the operands; determining if the live range of the operand (see col. 28, lines 1-62 regarding the live range of loop-variant variable) spans a function call; if so, attempting to allocate a preserved register (such as a static register 109 see Fig. 1; see also col. 28, lines 49-50); if not, attempting to allocate a scratch register (such as rotating register 107 see Fig. 1; see also col. 28, lines 60-61); and if the determination is unknown, treating the live range as tentative (see col. 29, lines 10-15); and if the allocation was successful, scheduling (by scheduler and register allocator 330, see Fig. 4; see also Col. 24, lines 30-45) the instruction. Note claims 12, and 23 recite the corresponding limitations as set forth in claim 1.

Referring to claim 35, Srinivasan'247 discloses, as claimed, a system (see Fig. 1) comprising: a set of instructions (inside such as processor 105, see Fig. 1) to be compiled; a set of preserved registers (such as a static register 109 see Fig. 1; see also col. 28, lines 49-50) capable of storing values that are to be preserved across function calls; a set of scratch registers (such as rotating register 107 see Fig. 1; see also col. 28, lines 60-61) capable to storing values that do not need

to be preserved across function calls; and an integrated compiler (optimizing compiler 100, see Fig. 2) having: an instruction scheduler (such as global scheduler 410 and modulo scheduler 420 which both are inside the scheduler and register allocator 330, see Fig. 4; see also Col. 24, lines 30-45) to: process a group of instructions in topological dependence order, and select an instruction, associated with at least one operand, to schedule an instruction, if the register allocation was successful; and a register allocator (such as rotating register allocator 530 see Fig. 6 which is inside the scheduler and register allocator 330, see Fig. 4; see also Col. 24, lines 30-45) to: allocate register to a live range associated with one or more operand, determine if the live range of the operand (see col. 28, lines 1-62 regarding the live range of loop-variant variable) spans a function call, if so, attempt to allocate a preserved register (such as a static register 109 see Fig. 1; see also col. 28, lines 49-50), if not, attempt to allocate a scratch register (such as rotating register 107 see Fig. 1; see also col. 28, lines 60-61), and if the determination is unknown, treat the live range as tentative (see col. 29, lines 10-15).

As to claims 2, 13, 24, and 36, Srinivasan'247 also disclose: the method of claim 1, wherein allocating a register to one or more of the operand includes: determining if the

operand's use begins a live range or ends a live range (see col. 28, lines 1-62 regarding the live range of loop-variant variable); if the operand's use begins a live range (see col. 28, lines 1-62 regarding the live range of loop-variant variable), attempting to allocate a register (such as a static register 109 or rotating register 107 see Fig. 1; see also col. 28, lines 49-50 or 60-61); if the operand's use ends a live range, marking the register associated with the operand as available for reallocation (see col. 28, lines 1-62 regarding the live range of loop-variant variable).

As to claims 3, 14, 25, and 37, Srinivasan'247 also disclose: the method of claim 1, wherein attempting to allocate a preserved register includes: determining if a preserved register (such as a static register 109 see Fig. 1; see also col. 28, lines 49-50) is available for allocation from a list of previously used preserved registers (the list inside the static registers 109 for indexing each registers); and if so, allocating the available preserved register for the live range defined by the operand (see col. 28, lines 1-62 regarding the operation relates to the live range of loop-variant variable).

As to claims 7, 18, 29, and 41, Srinivasan'247 also disclose: the method of claim 1, wherein treating the live range as tentative further includes: if both a scratch register and a

preserved register are available for allocation, reserving both the scratch register and the preserved register to the live range (see col. 28, lines 1-62 regarding the operation relates to the live range of loop-variant variable); allowing another instruction to be processed (this is the certain step for processing multiple instructions in the Srinivasan'247's system); and waiting for more information about the live range (see col. 28, lines 1-62 regarding the operation relates to the live range of loop-variant variable).

As to claims 11, 22, 33, and 45, Srinivasan'247 also disclose: the method of claim 1, wherein allocating a register to at least one or more of operands associated with the instruction includes: if no proper registers are available for allocation, inserting a register spill (see col. 28, lines 1-62 regarding the operation relates to the live range of loop-variant variable; note inserting a register spill is the certain step for using a limited registers inside the Srinivasan'247's system); and either re-attempting to allocate a register, or selecting another instruction to schedule (see col. 28, lines 1-62 regarding the operation relates to the live range of loop-variant variable).

As to claims 34, and 46, Srinivasan'247 also disclose: the apparatus of claim 23, wherein the register allocator includes:

a scratch register allocator (by scheduler and register allocator 330, see Fig. 4) to allocate scratch registers to live ranges that do not span a function call; a preserved register allocator (rotating register allocator 530, see Fig. 6) to allocate preserved registers to live ranges that span a function call; and a tentative register allocator (by scheduler and register allocator 330, see Fig. 4) to allocate either a scratch or a preserved register to live ranges that are not immediately known whether or not they span a function call (see col. 28, lines 1-62 regarding the operation relates to the live range of loop-variant variable).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chambers et al. discloses a system is disclosed that implements a declarative, annotation based dynamic compilation of the source code, employing a partial evaluation, binding-time analysis (BTA), and including program-point-specific polyvariant division and specialization and dynamic versions of traditional global and peephole optimizations.

Clarke discloses a method of compiling a computer program from a sequence of computer instructions including a plurality of first, set branch, instructions which each identify a target address for a branch and a plurality of associated second, effect branch instructions which each implement a branch to a target address.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Fritz M. Fleming, can be reached on (571) 272-4145. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

9. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This

practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
June 11, 2006